In the Abstract:

Please substitute the following abstract for the originally filed abstract:

Abstract of the Disclosure

Asynchronous memory devices utilize loopback circuitry to provide efficient and high speed "flow-through" of write data when conventional flow-through operations are not available. An exemplary memory device includes a memory array having first and second ports that can each support asynchronous read and write access and a first input/output control circuit. The first input/output control circuit is electrically coupled to the first port and includes a first sense amplifier, which is configured to receive read data from the first port, and a first bypass latch having an output coupled to the first sense amplifier. A second input/output control circuit is also provided. The second input/output control circuit is electrically coupled to the second port and includes a second sense amplifier, which is configured to receive read data from the second port, and a second bypass latch.